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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,855	02/17/2004	Gosagan Padmanabhan	852663.405	6239

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EXAMINER	
FENNEMA, ROBERT E	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/779,855	PADMANABHAN ET AL.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/07/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 are pending.

Claim Objections

2. Claim 1, line 2 ends in an unnecessary comma. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 5-10, 12-17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay et al. (US Patent Application Publication 2001/0010075, herein Tremblay), in view of Applicants admitted prior art (herein Padmanabhan).

5. As per Claim 1, Padmanabhan teaches: A microprocessor (Page 1, Line 12) comprising:

a memory array having a stack for saving contextual data (Page 1, Lines 16-17);

a central processing unit coupled to the memory array (Page 1, Line 13), the central processing unit having registers containing contextual data (Page 1, Lines 22-23) and a stack pointer (Page 2 Lines 19-23) and being arranged for saving contextual

data upon a switch from a first to a second program (Page 2, Lines 10-23), but fails to teach:

in a variable number of registers that varies according to the value of at least one flag stored in a register to be saved.

However, Tremblay teaches that as the number of registers increases in a machine, and the addressable memory size increases, the overhead for storing registers during a context switch increases, negatively impacting performance (Paragraphs 16-19). His solution is to create a dirty register, which stores dirty bits signifying if a register group has been updated, and thus needs to be stored to the stack, and on the context switch, only stores those groups (Paragraphs 20, 22, 23, and 72). This register and its flags are also saved in a history dirty register (Paragraph 106). Given this advantage of reducing the time of context switching and thus increasing performance, one of ordinary skill in the art at the time the invention was made would have implemented a dirty bit register to only store registers which had changed using Tremblay's method, in combination with the prior known method of context switching.

6. As per Claim 2, Tremblay teaches: The microprocessor according to claim 1 wherein the central processing unit is arranged for changing the value of the flag according to the content of a register, before saving contextual data contained in a variable number of registers that varies according to the value of the flag (Paragraphs 71-72) .

7. As per Claim 5, Tremblay teaches: The microprocessor according to claim 1 wherein the central processing unit is arranged for performing a test on the value of the flag so as to determine the number of registers to be saved (Paragraph 23).

8. As per Claim 6, Tremblay teaches: The microprocessor according to claim 1 wherein the central processing unit is arranged for, upon the return to the first program:

restoring the register containing the flag (Paragraph 106); and

restoring contextual data contained in a variable number of registers that varies according to the value of the flag present in the restored register (Paragraph 18, on a context switch, the incoming process has to bring it it's previously saved registers).

9. As per Claim 7, Tremblay teaches: The microprocessor according to claim 1 wherein the central processing unit is arranged for saving the register containing the flag last (Tremblay, Paragraph 106, and Padmanabhan Page 1, Lines 16-17).

10. As per Claim 8, Tremblay teaches: The microprocessor according to claim 1 wherein the flag comprises at least one bit of a register containing condition code flags (Paragraph 72).

11. As per Claim 9, Padmanabhan teaches: A method for managing the stack of a microprocessor having a central processing unit (Page 1, Line 13) and a memory array (Page 1, Lines 16-17), the central processing unit having registers containing contextual

data (Page 1, Lines 22-23) and a stack pointer (Page 2, Lines 19-23), the stack being a zone of the memory array dedicated to saving contextual data upon a switch from a first to a second program (Page 2, Lines 10-23), but fails to teach:

saving contextual data contained in a variable number of registers that varies according to the value of at least one flag stored in a register to be saved.

However, Tremblay teaches that as the number of registers increases in a machine, and the addressable memory size increases, the overhead for storing registers during a context switch increases, negatively impacting performance (Paragraphs 16-19). His solution is to create a dirty register, which stores dirty bits signifying if a register group has been updated, and thus needs to be stored to the stack, and on the context switch, only stores those groups (Paragraphs 20, 22, 23, and 72). This register and its flags are also saved in a history dirty register (Paragraph 106). Given this advantage of reducing the time of context switching and thus increasing performance, one of ordinary skill in the art at the time the invention was made would have implemented a dirty bit register to only store registers which had changed using Tremblay's method, in combination with the prior known method of context switching.

12. As per Claim 10, Tremblay teaches: The method according to claim 9, comprising a step of:

changing the value of the flag according to the content of a register, before saving contextual data contained in a variable number of registers that varies according

to the value of the flag (Paragraphs 71-72).

13. As per Claim 13, Tremblay teaches: The method according to claim 9, comprising a step of:

testing the value of the flag for determining the number of registers containing the data to be saved (Paragraph 23).

14. As per Claim 14, Tremblay teaches: The method according to claim 9, comprising the following steps:

restoring the register containing the flag (Paragraph 106); then

restoring contextual data contained in a variable number of registers that varies according to the value of the flag present in the restored register (Paragraph 18, on a context switch, the incoming process has to bring it it's previously saved registers).

15. As per Claim 15, Tremblay teaches: The method according to one claim 9 wherein the register containing the flag is saved last and is restored first (Tremblay, Paragraph 106, and Padmanabhan Page 1, Lines 16-17).

16. As per Claim 16, Tremblay teaches: The method according to claim 9 wherein the flag is formed by at least one bit of a register containing condition code flags (Paragraph 72).

17. As per Claim 17, Padmanabhan teaches: A microprocessor comprising:

a memory array having stored therein contextual data (Page 1, Lines 16-17);

a central processing unit coupled to the memory array (Page 1 Line 13);

a plurality of registers associated with the central processing unit (Page 1, Lines 22-23); and

a stack pointer associated with the central processing unit and being arranged for directing contextual data to be stored (Page 2, Lines 19-23), but fails to teach:

a first group of the registers storing contextual data and a second group of the registers not storing contextual data when a flag has a first value and switching to store contextual data also in the second group of registers when the flag switches to a second value, such that the number of registers that store contextual data is variable

a stack pointer associated with the central processing unit and being arranged for directing contextual data to be stored in the first group only or in both the second group and the first group, based on the flag value.

However, Tremblay teaches that as the number of registers increases in a machine, and the addressable memory size increases, the overhead for storing registers during a context switch increases, negatively impacting performance (Paragraphs 16-19). His solution is to create a dirty register, which stores dirty bits signifying if a register group has been updated, and thus needs to be stored to the stack, and on the context switch, only stores those groups (Paragraphs 20, 22, 23, and 72). This register and its flags are also saved in a history dirty register (Paragraph 106). Given this advantage of reducing the time of context switching and thus increasing

performance, one of ordinary skill in the art at the time the invention was made would have implemented a dirty bit register to only store registers which had changed using Tremblay's method, in combination with the prior known method of context switching.

18. As per Claim 19, Tremblay teaches: The microprocessor according to claim 17 wherein the second group of registers includes a single register (Column 23, the dirty bit can apply to either a group or a single register).

19. Claims 3-4, 11-12, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Padmanabhan and Tremblay, further in view of Kishida et al. (USPN 6,199,155, herein Kishida).

20. As per Claim 3, Padmanabhan and Tremblay teach the microprocessor according to claim 2, wherein the central processing unit is arranged for changing the value of the flag according to the content of a program counter of the central processing unit (Paragraph 72), but fails to teach:

an extended addressing register of a program counter of the central processing unit.

Tremblay teaches that a larger number of registers may be added to a system in order to increase performance in the machine, but has the drawback of the number of bits used in the instruction having to increase, and may cause additional problems (Paragraphs 16-18). Kishida teaches a system in which with a large number of

registers, two different addressing schemes can be used, one to address the small number of registers, and another scheme to be able to address the larger number of registers (Column 3, Lines 35-50). The advantage of this is being able to perform operations at a higher speed, without having to increase the code size (Column 3, Lines 48-50), which can increase the cost of the chip (Column 1, Lines 30-42). Given the advantage of increased performance and decreased cost, one of ordinary skill in the art at the time the invention was made would have been motivated to allow a user to select between two register sizes, one larger than the other, creating an extended addressing register for the larger of the two groups.

21. As per Claim 4, Tremblay teaches: The microprocessor according to claim 3 wherein the central processing unit is arranged for:

when the content of the extended addressing register is equal to 0, saving all the registers of the central processing unit containing contextual data, except for the extended addressing register (Paragraph 72); and

when the content of the extended addressing register is not equal to 0, saving all the registers of the central processing unit containing contextual data, including the extended addressing register (Paragraph 72).

22. As per Claim 11, Padmanabhan and Tremblay teach the method according to claim 10 wherein the value of the flag is changed according to the content of an

addressing register of a program counter of the central processing unit, but fails to teach: an extended addressing register of a program counter.

Tremblay teaches that a larger number of registers may be added to a system in order to increase performance in the machine, but has the drawback of the number of bits used in the instruction having to increase, and may cause additional problems (Paragraphs 16-18). Kishida teaches a system in which with a large number of registers, two different addressing schemes can be used, one to address the small number of registers, and another scheme to be able to address the larger number of registers (Column 3, Lines 35-50). The advantage of this is being able to perform operations at a higher speed, without having to increase the code size (Column 3, Lines 48-50), which can increase the cost of the chip (Column 1, Lines 30-42). Given the advantage of increased performance and decreased cost, one of ordinary skill in the art at the time the invention was made would have been motivated to allow a user to select between two register sizes, one larger than the other, creating an extended addressing register for the larger of the two groups.

23. As per Claim 12, Tremblay teaches: The method according to claim 11, comprising the following steps:

when the content of the extended addressing register is equal to 0, saving all the registers of the central processing unit containing contextual data, except for the extended addressing register (Paragraph 72); or

when the content of the extended addressing register is not equal to 0, saving all the registers of the central processing unit containing contextual data, including the extended addressing register (Paragraph 72).

24. As per Claim 18, Padmanabhan and Tremblay teach the microprocessor according to claim 17, but fail to teach:

wherein the second group of registers includes a register which is used as an extended addressing register when the flag is at a first value.

Tremblay teaches that a larger number of registers may be added to a system in order to increase performance in the machine, but has the drawback of the number of bits used in the instruction having to increase, and may cause additional problems (Paragraphs 16-18). Kishida teaches a system in which with a large number of registers, two different addressing schemes can be used, one to address the small number of registers, and another scheme to be able to address the larger number of registers (Column 3, Lines 35-50). The advantage of this is being able to perform operations at a higher speed, without having to increase the code size (Column 3, Lines 48-50), which can increase the cost of the chip (Column 1, Lines 30-42). Given the advantage of increased performance and decreased cost, one of ordinary skill in the art at the time the invention was made would have been motivated to allow a user to select between two register sizes, one larger than the other, creating an extended addressing register for the larger of the two groups.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

26. Shaylor (USPN 6,408,325) teaches a method for context switching in a system with large register files.

27. Damron (US Patent Application Publication 2004/0003208) teaches a system of marking registers with a valid bits between context switches.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert E Fennema
Examiner
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